

REMARKS

Applicants thank the Examiner for her Office Action dated July 7th, 2003 in relation to this patent application.

Without conceding the propriety of the Examiner's position, and solely to expedite prosecution, claims 10-12 have been cancelled without prejudice or disclaimer.

Applicants respectfully request reconsideration of the Prior Art (§ 102) and Obviousness (§ 103) rejections set forth by the Examiner under 35 U.S.C. in light of the currently amended claims.

Examiners' claims of Prior Art have been overcome by the addition of language to claims 1 – 5, and 13-15 that more accurately labels the novelty of the current invention. In addition, the language of claims 13 and 14 has been modified to make the claimed method clearer to the examiner.

Claims 1-5 and 13-15 have been amended to identify the advantage of the current invention over the cited Prior Art. We have narrowed the language of the claims from utilizing a “field effect transistor” to a “hetero-junction field effect transistor.” In addition, we have narrowed the language of the claims from that of a “diode” to a “Schottky barrier diode.” The advantage of the current invention is that the fabrication of the hetero-junction FET can be created using the same process step as the fabrication of the Schottky barrier diode. As a result, we can create a semiconductor utilizing hetero-junction semiconductor technology with the addition of a protection circuit that, by design, advantageously minimizes leakage current by using a plurality of protection diodes, all without increasing the number of steps in the process and without restricting the pattern layout of the HFET. Neither Voldman nor Tsuzuki, considered together or alone, teach or suggest the advantages inherent in the present invention.

Accordingly, Applicants' invention is patentable and distinct over the art of record.
In light of the foregoing, Applicants respectfully submit that all claims now stand in
condition for allowance.

Respectfully submitted,

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